

Operation	§	Assembler	Action	Notes
Load	with immediate offset, word	LDR Rd, [Rn, #<immed>]	Rd := [Rn + immed]	Immediate range 0-124, multiple of 4.
	halfword	LDRH Rd, [Rn, #<immed>]	Rd := ZeroExtend([Rn + immed][15:0])	Clears bits 31:16. Immediate range 0-62, even.
	byte	LDRB Rd, [Rn, #<immed>]	Rd := ZeroExtend([Rn + immed][7:0])	Clears bits 31:8. Immediate range 0-31.
	with register offset, word	LDR Rd, [Rn, Rm]	Rd := [Rn + Rm]	
	halfword	LDRH Rd, [Rn, Rm]	Rd := ZeroExtend([Rn + Rm][15:0])	Clears bits 31:16
	signed halfword	LDRSH Rd, [Rn, Rm]	Rd := SignExtend([Rn + Rm][15:0])	Sets bits 31:16 to bit 15
	byte	LDRB Rd, [Rn, Rm]	Rd := ZeroExtend([Rn + Rm][7:0])	Clears bits 31:8
	signed byte	LDRSB Rd, [Rn, Rm]	Rd := SignExtend([Rn + Rm][7:0])	Sets bits 31:8 to bit 7
PC-relative	LDR Rd, [PC, #<immed>]	Rd := [(R15 AND 0xFFFFF0) + immed]	Immediate range 0-1020, multiple of 4.	
SP-relative	LDR Rd, [SP, #<immed>]	Rd := [R13 + immed]	Immediate range 0-1020, multiple of 4.	
Multiple	LDMIA Rn!, <reglist>	Loads list of registers	Always updates base register.	
Store	with immediate offset, word	STR Rd, [Rn, #<immed>]	[Rn + immed] := Rd	Immediate range 0-124, multiple of 4.
	halfword	STRH Rd, [Rn, #<immed>]	[Rn + immed][15:0] := Rd[15:0]	Ignores Rd[31:16]. Immediate range 0-62, even.
	byte	STRB Rd, [Rn, #<immed>]	[Rn + immed][7:0] := Rd[7:0]	Ignores Rd[31:8]. Immediate range 0-31.
	with register offset, word	STR Rd, [Rn, Rm]	[Rn + Rm] := Rd	
	halfword	STRH Rd, [Rn, Rm]	[Rn + Rm][15:0] := Rd[15:0]	Ignores Rd[31:16]
	byte	STRB Rd, [Rn, Rm]	[Rn + Rm][7:0] := Rd[7:0]	Ignores Rd[31:8]
	SP-relative, word	STR Rd, [SP, #<immed>]	[R13 + immed] := Rd	Immediate range 0-1020, multiple of 4.
Multiple	STMIA Rn!, <reglist>	Stores list of registers	Always updates base register.	
Push/Pop	Push	PUSH <loregrlist>	Push registers onto stack	Full descending stack.
	Push with link	PUSH <loregrlist+LR>	Push LR and registers onto stack	
	Pop	POP <loregrlist>	Pop registers from stack	
	Pop and return	4T POP <loregrlist+PC>	Pop registers, branch to address loaded to PC	
	Pop and return with exchange	5T POP <loregrlist+PC>	Pop, branch, and change to ARM state if address[0] = 0	
Branch	Conditional branch	B{cond} label	R15 := label	label must be within -252 to +258 bytes of current instruction. See Table Condition Field on reverse.
	Unconditional branch	B label	R15 := label	label must be within ±2Kb of current instruction.
	Long branch with link	BL label	R14 := address of next instruction, R15 := label	Encoded as two Thumb instructions.
	Branch and exchange	BX Rm	R15 := Rm AND 0xFFFFF0	label must be within ±4Mb of current instruction.
	Branch with link and exchange	5T BLX label	R14 := address of next instruction, R15 := label Change to ARM	Change to ARM state if Rm[0] = 0. Encoded as two Thumb instructions.
Branch with link and exchange	5T BLX Rm	R14 := address of next instruction, R15 := Rm AND 0xFFFFF0	label must be within ±4Mb of current instruction. Change to ARM state if Rm[0] = 0	
Extend	Signed extend halfword to word	6 SXTB Rd, Rm	Rd[31:0] := SignExtend(Rm[15:0])	
	Signed extend byte to word	6 SXTB Rd, Rm	Rd[31:0] := SignExtend(Rm[7:0])	
	Unsigned extend halfword to word	6 UXTH Rd, Rm	Rd[31:0] := ZeroExtend(Rm[15:0])	
	Unsigned extend byte to word	6 UXTB Rd, Rm	Rd[31:0] := ZeroExtend(Rm[7:0])	
Processor state change	Software interrupt	6 SWI <immed_8>	Software interrupt processor exception	8-bit immediate value encoded in instruction.
	Change processor state	6 CPSID <iflags>	Disable specified interrupts	
		6 CPSIE <iflags>	Enable specified interrupts	
	Set endianness	6 SETEND <endianness>	Sets endianness for loads and saves.	<endianness> can be BE (Big Endian) or LE (Little Endian).
	Breakpoint	5T BKPT <immed_8>	Prefetch abort <i>or</i> enter debug state	8-bit immediate value encoded in instruction.

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Quick Reference Card

Key to Tables	{cond} <S/D> <S/D/X> <VFPsysreg>	See Table Condition Field S (single precision) or D (double precision). As above, or X (unspecified precision). FPSCR, or FPSID.
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Fd, Fn, Fm {E} {Z} <VFPregs>	Sd, Sn, Sm (single precision), or Dd, Dn, Dm (double precision). E : raise exception on any NaN. Without E : raise exception only on signaling NaNs. Round towards zero. Overrides FPSCR rounding mode. A comma separated list of <i>consecutive</i> VFP registers, enclosed in braces ({ and }).
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Operation	Assembler	Exceptions	Action	Notes													
Vector arithmetic	Multiply	FMUL<S/D>{cond} Fd, Fn, Fm	IO, OF, UF, IX	Fd := Fn * Fm	<table border="1"> <thead> <tr> <th colspan="2">Exceptions</th> </tr> </thead> <tbody> <tr> <td>IO</td> <td>Invalid operation</td> </tr> <tr> <td>OF</td> <td>Overflow</td> </tr> <tr> <td>UF</td> <td>Underflow</td> </tr> <tr> <td>IX</td> <td>Inexact result</td> </tr> <tr> <td>DZ</td> <td>Division by zero</td> </tr> </tbody> </table>	Exceptions		IO	Invalid operation	OF	Overflow	UF	Underflow	IX	Inexact result	DZ	Division by zero
	Exceptions																
	IO	Invalid operation															
	OF	Overflow															
	UF	Underflow															
	IX	Inexact result															
	DZ	Division by zero															
	and negate	FNMUL<S/D>{cond} Fd, Fn, Fm	IO, OF, UF, IX	Fd := - (Fn * Fm)													
	and accumulate	FMAC<S/D>{cond} Fd, Fn, Fm	IO, OF, UF, IX	Fd := Fd + (Fn * Fm)													
	negate and accumulate	FNMAC<S/D>{cond} Fd, Fn, Fm	IO, OF, UF, IX	Fd := Fd - (Fn * Fm)													
	and subtract	FMSC<S/D>{cond} Fd, Fn, Fm	IO, OF, UF, IX	Fd := - Fd + (Fn * Fm)													
negate and subtract	FNMSC<S/D>{cond} Fd, Fn, Fm	IO, OF, UF, IX	Fd := - Fd - (Fn * Fm)														
Add	FADD<S/D>{cond} Fd, Fn, Fm	IO, OF, IX	Fd := Fn + Fm														
Subtract	FSUB<S/D>{cond} Fd, Fn, Fm	IO, OF, IX	Fd := Fn - Fm														
Divide	FDIV<S/D>{cond} Fd, Fn, Fm	IO, DZ, OF, UF, IX	Fd := Fn / Fm														
Copy	FCPY<S/D>{cond} Fd, Fm		Fd := Fm														
Absolute	FABS<S/D>{cond} Fd, Fm		Fd := abs(Fm)														
Negative	FNEG<S/D>{cond} Fd, Fm		Fd := - Fm														
Square root	FSQRT<S/D>{cond} Fd, Fm	IO, IX	Fd := sqrt(Fm)														
Scalar compare	Two values	FCMP{E}<S/D>{cond} Fd, Fm	IO	Set FPSCR flags on Fd - Fm	Use FMSTAT to transfer flags.												
	Value with zero	FCMP{E}Z<S/D>{cond} Fd	IO	Set FPSCR flags on Fd - 0	Use FMSTAT to transfer flags.												
Scalar convert	Single to double	FCVTDS{cond} Dd, Sm	IO	Dd := convertStoD(Sm)													
	Double to single	FCVTSD{cond} Sd, Dm	IO, OF, UF, IX	Sd := convertDtoS(Dm)													
	Unsigned integer to float	FUITO<S/D>{cond} Fd, Sm	IX	Fd := convertUItoF(Sm)													
	Signed integer to float	FSITO<S/D>{cond} Fd, Sm	IX	Fd := convertSIttoF(Sm)													
	Float to unsigned integer	FTOUI{Z}<S/D>{cond} Sd, Fm	IO, IX	Sd := convertFtoUI(Fm)													
	Float to signed integer	FTOSI{Z}<S/D>{cond} Sd, Fm	IO, IX	Sd := convertFtoSI(Fm)													
Save VFP registers		FST<S/D>{cond} Fd, [Rn{, #<immed>}]		[address] := Fd. Immediate range 0-1020, multiple of 4.													
	Multiple, unindexed increment after decrement before	FSTMIA<S/D/X>{cond} Rn, <VFPregs> FSTMIA<S/D/X>{cond} Rn!, <VFPregs> FSTMDB<S/D/X>{cond} Rn!, <VFPregs>		Saves list of VFP registers, starting at address in Rn. synonym: FSTMIA (empty ascending) synonym: FSTMFD (full descending)													
Load VFP registers		FLD<S/D>{cond} Fd, [Rn{, #<immed>}]		Fd := [address]. Immediate range 0-1020, multiple of 4.													
	Multiple, unindexed increment after decrement before	FLDMIA<S/D/X>{cond} Rn, <VFPregs> FLDMIA<S/D/X>{cond} Rn!, <VFPregs> FLDMDB<S/D/X>{cond} Rn!, <VFPregs>		Loads list of VFP registers, starting at address in Rn. synonym: FLDMFD (full descending) synonym: FLDMIA (empty ascending)													
Transfer registers	ARM to single	FMSR{cond} Sn, Rd		Sn := Rd													
	Single to ARM	FMRS{cond} Rd, Sn		Rd := Sn													
	Two ARM to two singles	FMSRR{cond} {Sn,Sm}, Rd, Rn		Sn := Rd, Sm := Rn	Architecture VFPv2 only												
	Two singles to two ARM	FMRRS{cond} Rd, Rn, {Sn,Sm}		Rd := Sn, Rn := Sm	Architecture VFPv2 only												
	Two ARM to double	FMDRR{cond} Dn, Rd, Rn		Dn[31:0] := Rd, Dn[63:32] := Rn	Architecture VFPv2 only												
	Double to two ARM	FMRRD{cond} Rd, Rn, Dn		Rd := Dn[31:0], Rn := Dn[63:32]	Architecture VFPv2 only												
	ARM to lower half of double	FMDLR{cond} Dn, Rd		Dn[31:0] := Rd	Use with FMDHR.												
	Lower half of double to ARM	FMRDL{cond} Rd, Dn		Rd := Dn[31:0]	Use with FMRDH.												
	ARM to upper half of double	FMDHR{cond} Dn, Rd		Dn[63:32] := Rd	Use with FMDLR.												
	Upper half of double to ARM	FMRDH{cond} Rd, Dn		Rd := Dn[63:32]	Use with FMRDL.												
	ARM to VFP system register	FMXR{cond} <VFPsysreg>, Rd		VFPsysreg := Rd	Stalls ARM until all VFP ops complete.												
	VFP system register to ARM	FMRX{cond} Rd, <VFPsysreg>		Rd := VFPsysreg	Stalls ARM until all VFP ops complete.												
	FPSCR flags to CPSR	FMSTAT{cond}		CPSR flags := FPSCR flags	Equivalent to FMRX R15, FPSCR												

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FPSCR format								Rounding		(Stride - 1)*3		Vector length - 1				Exception trap enable bits						Cumulative exception bits								
31	30	29	28				24	23	22	21	20		18	17	16			12	11	10	9	8				4	3	2	1	0
N	Z	C	V				FZ	RMODE		STRIDE			LEN			IXE	UFE	OFE	DZE	IOE				IXC	UFC	OFC	DZC	IOC		
FZ: 1 = flush to zero mode.								Rounding: 0 = round to nearest, 1 = towards +∞ 2 = towards -∞ 3 = towards zero.						(Vector length * Stride) must not exceed 4 for double precision operands.																

If Fd is S0-S7 or D0-D3, operation is Scalar (regardless of vector length).	If Fd is S8-S31 or D4-D15, and Fm is S0-S7 or D0-D3, operation is Mixed (Fm scalar, others vector).
If Fd is S8-S31 or D4-D15, and Fm is S8-S31 or D4-D15, operation is Vector.	S0-S7 (or D0-D3), S8-S15 (D4-D7), S16-S23 (D8-D11), S24-S31 (D12-D15) each form a circulating bank of registers.

Condition Field		
Mnemonic	Description (Thumb)	Description (VFP)
EQ	Equal	Equal
NE	Not equal	Not equal, or unordered
CS / HS	Carry Set / Unsigned higher or same	Greater than or equal, or unordered
CC / LO	Carry Clear / Unsigned lower	Less than
MI	Negative	Less than
PL	Positive or zero	Greater than or equal, or unordered
VS	Overflow	Unordered (at least one NaN operand)
VC	No overflow	Not unordered
HI	Unsigned higher	Greater than, or unordered
LS	Unsigned lower or same	Less than or equal
GE	Signed greater than or equal	Greater than or equal
LT	Signed less than	Less than, or unordered
GT	Signed greater than	Greater than
LE	Signed less than or equal	Less than or equal, or unordered
AL	Do not use in Thumb	Always (normally omitted)

Exceptions	
IO	Invalid operation
OF	Overflow
UF	Underflow
IX	Inexact result
DZ	Division by zero

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Change Log

Issue	Date	By	Change
A	June 1995	BJH	First Release
B	Sept 1996	BJH	Second Release
C	Nov 1998	BJH	Third Release
D	Oct 1999	CKS	Fourth Release
E	Oct 2000	CKS	Fifth Release
F	Sept 2001	CKS	Sixth Release
G	Jan 2003	CKS	Seventh Release
H	Oct 2003	CKS	Eighth Release